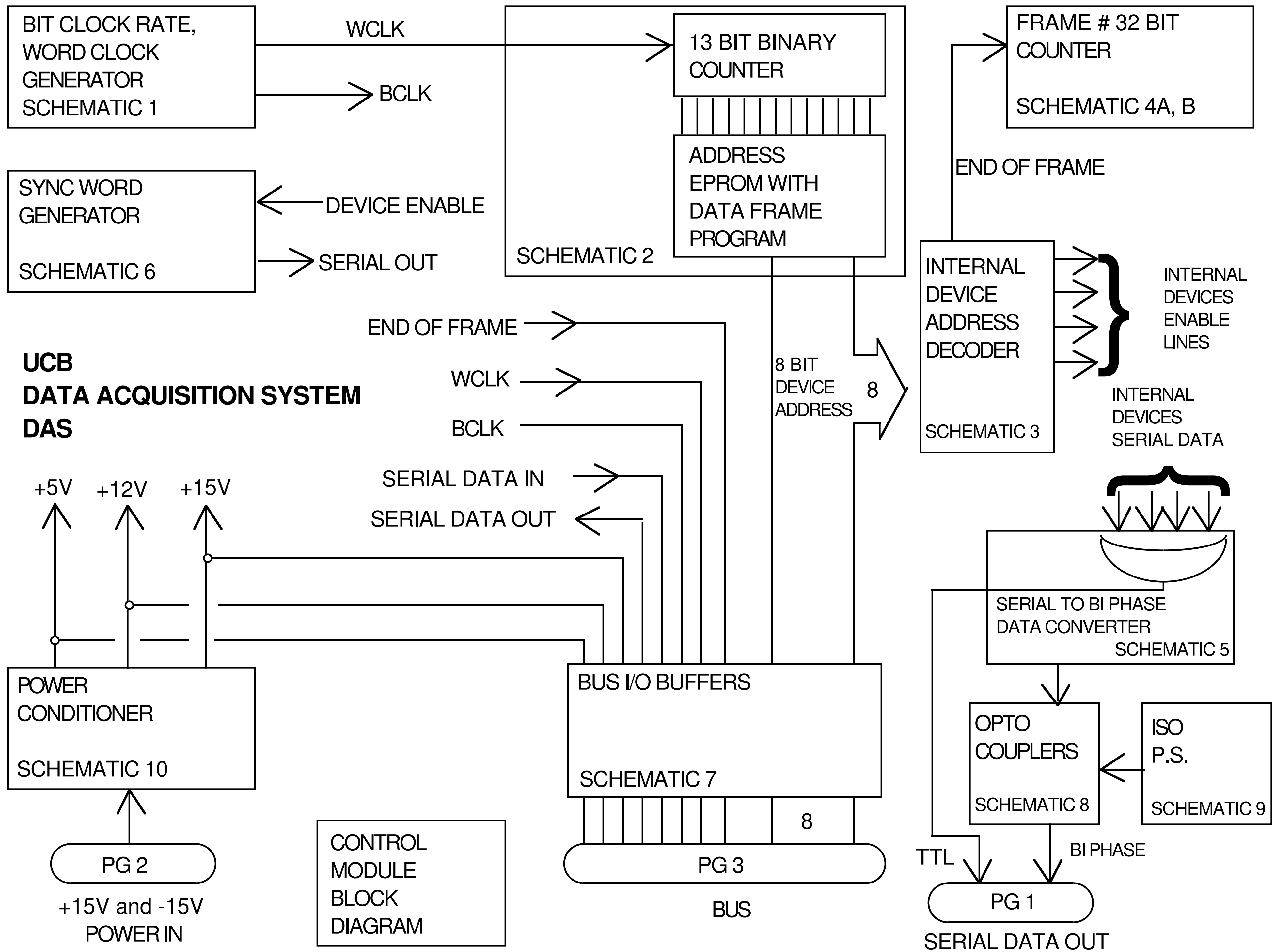

BIT CLOCK RATE,
WORD CLOCK
GENERATOR
SCHEMATIC 1
WCLK
BCLK
13 BIT BINARY
COUNTER
ADDRESS
EPROM WITH
DATA FRAME
PROGRAM
SCHEMATIC 2
FRAME # 32 BIT
COUNTER
SCHEMATIC 4A, B
END OF FRAME
SYNC WORD
GENERATOR
SCHEMATIC 6
DEVICE ENABLE
SERIAL OUT
INTERNAL
DEVICE
ADDRESS
DECODER
SCHEMATIC 3
INTERNAL
DEVICES
ENABLE
LINES
END OF FRAME
WCLK
BCLK
8 BIT
DEVICE
ADDRESS
8
INTERNAL
DEVICES
SERIAL DATA
UCB
DATA ACQUISITION SYSTEM
DAS
SERIAL DATA IN
SERIAL DATA OUT
+5V
+12V
+15V
SERIAL TO BI PHASE
DATA CONVERTER
SCHEMATIC 5
POWER
CONDITIONER
SCHEMATIC 10
BUS I/O BUFFERS
SCHEMATIC 7
OPTO
COUPLERS
SCHEMATIC 8
ISO
P.S.
SCHEMATIC 9
8
PG 2
+15V and -15V
POWER IN
CONTROL
MODULE
BLOCK
DIAGRAM
PG 3
BUS
TTL
BI PHASE
PG 1
SERIAL DATA OUT